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thickness.

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## What is claimed:

1	1. A semiconductor device comprising:
2	a pad which is formed on an insulating layer and has an electric connection region
3	to connect with external components; and
4	a protective insulating layer which is formed on the insulating layer and the pad and
5	has an aperture for exposing the electric connection region,
6	wherein at least part of a side surface of the protective insulating layer surrounding
7	the electric connection region is a tapered surface with an acute angle to a top surface of the
8	pad; and
9	wherein the protective insulating layer includes at least first and second insulating
10	layers, each of which has a side surface exposed to the aperture.
1	2. The semiconductor device of claim 1,
2	wherein an etching rate of a material forming the first insulating layer is different
3	from an etching rate of a material forming the second insulating layer.
1	3. The semiconductor device of claim
2	wherein the first insulating layer is formed on the insulating layer; and
3	wherein the second insulating layer is formed on the first insulating layer.
1	4. The semiconductor device of claim 1,
2	wherein the second insulating layer is larger than the first insulating layer in

- The semiconductor device of claim 4, 5. 1
- wherein the first insulating layer has a thickness of 400 nm to 600 nm; and 2
- wherein the second insulating layer has a thickness of 600 nm to 1400 nm. 3

1	6.	The	semicd	nductor	device	of claim	1,

- wherein at least the side surface of the second insulating layer exposed to the
- aperture is a tapered surface with an acute angle to the top surface of the pad.
- 1 7. The semiconductor device of claim 1,
- wherein a tapered angle between the side surface of the second insulating layer
- 3 exposed to the aperture and the top surface of the pad is smaller than a tapered angle
- between a side surface of the first insulating layer exposed to the aperture and the top
- 5 surface of the pad.
- 1 8. The semiconductor device of claim/1
- wherein a tapered angle between the side surface of a portion of the second
- insulating layer exposed to the aperture and the top sufface of the pad is in the range of 30°
- 4 to 60°.
- 1 9. The semiconductor device of claim 1,
- wherein an angle between the side surface of a portion of the first insulating layer
- 3 exposed to the aperture and the top surface of the pad is in the range of 60° to 90°.
- 1 10. The semiconductor device of claim 1,
- wherein the distance between an upper end of the side surface of the first insulating
- 3 layer exposed to the aperture and a lower end of the side surface of the second insulating
- 4 layer exposed to the aperture is in the range of 0  $\mu$ m to 3  $\mu$ m.
- 1 11. The semiconductor device of claim  $\lambda_0$ ,
- wherein the distance is in the range of  $0 \mu m$  to  $1 \mu m$ .

1 12. The semidonauctor device of claim		12.	The semidonductor device of claim	i	1
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- wherein the aperture in the second insulating layer is larger than the aperture in the
- 3 first insulating layer
- 1 13. The semiconductor device of claim 1,
- wherein a bump electrode is formed on the electric connection region in the pad
- 3 through a barrier layer.
- 1 14. The semiconductor device of claim 1,
- wherein the first and second insulating layer are patterned by means of the same
- 3 mask layer.
- 1 15. The semiconductor device of claim 1,
- wherein the first insulating layer is formed of a silicon oxide layer.
- 1 16. The semiconductor device of claim 1.
- wherein the second insulating layer is formed of a silicon nitride layer.
- 1 17. A semiconductor device comprising:
- a pad which is formed on an insulating layer and includes an electric connection
- 3 region with external components; and
- a protective insulating layer which is formed on the insulating layer and the pad and
- 5 includes an aperture over at least part of the electric connection region,
- 6 wherein a side surface of the protective insulating layer surrounding the electric
- 7 connection region is a tapered surface with an acute angle to a top surface of the pad.
- 1 18. The semiconductor device of claim 17,
- wherein the protective insulating layer has a thickness of 1000 nm to 2000 nm.

1	10	The sen	nibonductor	device	of claim	17
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- wherein a tapered angle between the side surface of the second insulating layer
- 3 surrounding the electric connection region and the top surface of the pad is in the range of
- 4 10° to 80°.
- 1 20. The semiconductor device of claim 17,
- wherein a bump electrode is provided on the electric connection region of the pad
- 3 through a barrier layer.
- 1 21. The semiconductor device of claim 17,
- wherein the protective insulating layer is formed of one of a silicon oxide layer and
- 3 a silicon nitride layer.
- 1 22. A method of fabricating a senticonductor device comprising:
- forming a pad with a predetermined pattern-on an insulating layer;
- forming a protective insulating layer on the insulating layer and over the pad by
- 4 sequentially forming at least first and second insulating layers;
- forming a mask layer on the protective insulating layer, the mask layer having an
- 6 aperture in a region corresponding to an electric connection region of the pad; and
- 7 selectively etching the first and second insulating layers by using the mask layer as
- 8 a mask to expose the electric connection region.
- 1 23. The method of fabricating a semiconductor device of claim 22,
- wherein the second insulating layer is patterned by isotropic etching.
- 1 24. The method of fabricating a semiconductor device of claim 22,
- wherein the first insulating layer is patterned by anisotropic etching.

1	25.	The metho	d of fabricating a	semiconductor	device of	claim 22,
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- wherein the first and second insulating layers are continuously patterned.
- 1 26. The method of fabricating a semiconductor device of claim 22,
- wherein an etching rate of a material forming the first insulating layer is different
- 3 from an etching rate of a material forming the second insulating layer.
- 1 27. The method of fabricating a semiconductor device of claim 22,
- wherein the second insulating layer is larger than the first insulating layer in
- 3 thickness.
- 1 28. The method of fabricating a semiconfluctor device of claim 27,
- wherein the first insulating layer has a thickness of 400 nm to 600 nm; and
- wherein the second insulating layer has a thickness of 600 nm to 1400 nm.
- 1 29. The method of fabricating a semiconductor device of claim 22,
- wherein at least a side surface of the second insulating layer surrounding the
- 3 electric connection region has a tapered surface with an acute angle to the top surface of the
- 4 pad.
- 1 30. The method of fabricating a semiconductor device of claim 22,
- wherein a tapered angle between the side surface of the second insulating layer
- 3 surrounding the electric connection region and the top surface of the pad is smaller than a
- 4 tapered angle between the side surface of the first insulating layer surrounding the electric
- 5 connection region and the top surface of the pad.

- 1 31. The method of fabricating a semiconductor device of claim 22,
- wherein a tapered angle between the side surface of a portion of the second
- 3 insulating layer surrounding the electric connection region and the top surface of the pad is
- 4 in the range of 30° to 60°.
- 1 32. The method of fabricating a semiconductor device of claim 22,
- wherein an angle between the side surface of a portion of the first insulating layer
- 3 surrounding the electric connection region and the top surface of the pad is in the range of
- 4 60° to 90°.
- 1 33. The method of fabricating a semiconductor device of claim 22,
- wherein the distance between an upper end of the side surface of the first insulating
- 3 layer surrounding the electric connection region and a lower end of the side surface of the
- 4 second insulating layer surrounding the electric connection region is in the range of 0 μm to
- 5 3 μm.
- 1 34. The method of fabricating a semiconductor device of claim 33,
- wherein the distance is in the range of 0  $\mu$ m to 1  $\mu$ m.
- 1 35. The method of fabricating a semiconductor device of claim 22,
- wherein the aperture in the second insulating layer is larger than the aperture in the
- 3 first insulating layer.
- 1 36. The method of fabricating a semiconductor device of claim 22,
- wherein a bump electrode is formed on the electric connection region in the pad
- 3 through a barrier layer.
- 1 37. The method of fabricating a semiconductor device of claim 22,
- wherein the first insulating layer is a silicon oxide layer.

1	38.	The method of	f fabricating a	semiconductor	device of	f claim 22,
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- wherein the second insulating layer is a nitride oxide layer.
- 1 39. A method of fabricating a semiconductor device comprising:
- 2 forming a pad with a predetermined pattern on an insulating layer;
- forming a protedtive insulating layer on the insulating layer over the pad;
- forming a mask layer on the protective insulating layer, the mask layer having an
- 5 aperture in a region corresponding to an electric connection region of the pad; and
- 6 patterning the projective insulating layer by isotropic etching with the mask layer as
- 7 a mask to expose the electric connection region.

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- 1 40. The method of fabricating a semiconductor device of claim 39,
- wherein the protective insulating layer has a thickness of 1000 nm to 2000 nm.
- 1 41. The method of fabricating a semiconductor device of claim 39,
- wherein a tapered angle between a side surface of the insulating layer surrounding
- 3 the electric connection region and the top surface of the pad is in the range of 10° to 80°.
- 1 42. The method of fabricating a semiconductor device of claim 39,
- wherein a bump electrode is provided on the electric connection region of the pad
- 3 through a barrier layer.
- 1 43. The method of fabricating a semiconductor device of claim 39,
- wherein the protective insulating layer is formed from a material including one of a
- 3 silicon oxide layer and a silicon hitride layer.

- 1 44. A bonding pad structure comprising:
- a bonding pad formed over a portion of a substrate;
- an insulating region formed over a portion of said bonding pad, wherein the
- 4 bonding pad includes an area surrounded by and uncovered by the insulating region;
- 5 the insulating region including a side surface surrounding the uncovered area of the
- bonding pad, wherein at least part of the side-surface is tapered and has an acute angle to a
- 7 top surface of the bonding pad.
- 1 45. The bonding pad structure of claim 44, wherein the insulating region comprises an
- 2 upper layer and a lower layer, and the side surface includes an upper layer side surface
- 3 having an acute angle to a top surface of the bonding pad and a lower layer side surface
- 4 having an acute angle to a top surface of the bonding pad.
- 1 46. The bonding pad structure of claim 45, wherein the upper layer side surface has an
- 2 angle of 30° to 60° to a surface parallel to a top surface of the bonding pad and the lower
- 3 side surface has an angle of 60° to 90° to a top surface of the bonding pad.
- 1 47. The bonding pad of structure of claim 44, wherein the at least part of the side
- 2 surface has an angle of 10° to 80° to an upper surface of said bonding pad.

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